UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/021,565	12/11/2001	Gregory M. Allen	04356.011 (P 0768)	9302

21681 7590 12/17/2004

PARSONS BEHL & LATIMER
ONE UTAH CENTER
201 SOUTH MAIN STREET SUITE 1800
SALT LAKE CITY, UT 84145-0898

EXAMINER	
HENRY, MATTHEW ALLAN	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/021,565	ALLEN ET AL.	
	Examiner	Art Unit	
	Matthew A. Henry	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☒ Claim(s) *1, 6, 18 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Figure 1, Item 44, Figure 4, Items 132 and 134, Figure 5, Items 152 and 154.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "54" in Figure 1 has been used to designate both an input buffer in Paragraph 29, Line 3 and a logic circuit in Paragraph 35, Line 3.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "38" in Figure 1 has been used to designate both an input buffer in Paragraph 32, Line 3 and ATA_EN in Paragraph 30, Line 1.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "58" in Figure 1 has been used to designate both an input buffer in Paragraph 30, Line 4 and the D- line in Paragraph 36, Line 6.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "106" in Figure 2 has been used to designate both the conditional branch "Is VBUS high" and the definite action "Disable pull-up resistor."

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page

header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

6. Claims 1, 6, 18 and 27 are objected to because of the following informalities:

Claim 1, Line 9 makes reference to an "integrate circuit." "integrate" should be replaced with "integrated" to be correct.

Claim 6, Line 1 states "said resistor comprises and NPN bipolar junction transistor." Resistors cannot be composed of transistors; it will be considered for the remainder of this Office Action that the word "resistor" should read "transistor."

Claim 18, Line 3 makes reference to an "integrate circuit." "integrate" should be replaced with "integrated" to be correct.

Claim 27, Line 1 makes reference to a "resister." "resister" should be replaced with "resistor" to be correct.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. **Claims 9 and 18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.** The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the

art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

9. Claims 9 and 18 cite an electrostatic protection diode coupled to a transistor such that the transistor may protect the electrostatic protection diode. The specification provides no explanation as to how the transistor provides this protection.

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 10, 13 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. Claim 13 recites the limitation "application specific integrated circuit" in Lines 1-2. There is insufficient antecedent basis for this limitation in the claim in that an integrated circuit rather than an application specific integrated circuit has been previously stated in the claim

For the purposes of examination the application specific integrated circuit will be interpreted to be an integrated circuit.

Regarding claims 10 and 22, the phrase "relatively little" renders the claim indefinite because it is unclear to what the relativity may be associated. See MPEP § 2173.05(f).

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

14. Claims 1, 7, 8, 10, 11, 15-19, 22, 25 and 29-31 are rejected under 35 U.S.C. 102(a) as being anticipated by Mariaud.

The prior art of reference is the French patent FR2817051A1, however the English language translation, U.S. Patent Publication 2002/0062456 will be made reference to herein.

Concerning Claim 1, Mariaud discloses:

An circuit for disabling a pull-up resistor connected to a data line of a universal serial bus device, comprising:

a universal serial bus connection (Figure 1, Item 24) comprised of at least one power source (Figure 1, Item 16) and at least two data lines (Figure 1, Items 12 and 14);

an integrated circuit (Figure 6) connected to the at least two data lines (The details of the data line connections are not shown, however connection to the data lines is considered inherent to the system because the absence of this connection would render the USB device incapable of data transfer) and having an input (Figure 6, Item 26; Paragraph, Lines 8-10);

an external power supply connected to the integrated circuit (Figure 3, Item 28);

at least one transistor interconnected between VBUS and the input (Figure 6, Items 26), the power source and the integrated circuit for controlling voltage to the input of the integrated circuit corresponding to the voltage of VBUS (Paragraph 6, Lines 1-6); and

a pull-up resistor connected between the application specific integrated circuit and a data line of a USB connection (Figure 1, Item Rr), the state of the pull-up being controlled by the application specific integrated circuit depending upon the voltage on the input (Paragraph 6, Lines 1-6).

Concerning Claim 7, Mariaud discloses:

circuitry for providing hysteresis to filter noise from the external power supply (Figure 6, Item 30; Paragraph 8, Lines 2-7).

Concerning Claim 8, Mariaud discloses:

the circuitry for providing hysteresis comprises an input buffer through which voltage on the input is buffered (Figure 6, Item 30; Paragraph 8, Lines 2-7).

Concerning Claim 10, Mariaud discloses:

The power supply source 26 is derived either from the voltage Vbus or from an external voltage Vdd at an input terminal 28 (Column 1, Lines 5-7).

Mariaud does not specifically disclose:

relatively little current is drawn from the power source when the external power supply is at zero.

However, a USB device inherently will be current limited in the absence of an external power supply and thus the current drawn will be 'relatively little.'

Concerning Claim 11, Mariaud discloses:

a logic circuit within the integrated circuit (Figure 6, Items 72 or 74).

Concerning Claim 15, Mariaud discloses:

A method of disabling a pull-up resistor connected to a data line of a universal serial bus device comprising a universal serial bus connection (Figure 1, Item 24) comprised of a power source (Figure 1, Item 16), at least two data lines (Figure 1, Items 12 and 14), a pull-up resistor connected to one of the at least two data lines (Figure 1, Item Rr), an external power supply (Figure 3, Item 28) and an integrated circuit having an input (Figure 6, Item 26; Paragraph 26, Lines 8-10), the method comprising:

detecting the presence of a voltage of the at least one power source (Figure 6, Item 60; Paragraph 25);

applying a voltage to the input of the integrated circuit that is proportionate to the voltage on the at least one power supply (Paragraph 25);

determining if the voltage on the input represents a logic one or a logic zero (Figure 6, Item 26; Paragraph 8, Lines 2-7); and

enabling the pull-up resistor if the voltage on the input represents a logic one and disabling the pull-up resistor if the voltage on the input represents a logic zero (Figure 6, item 26; Paragraph 8, Lines 7-11).

Concerning Claim 16, Mariaud discloses:

preventing the pull-up resistor from alternating from enabled to disabled due to noise in a signal from the external power supply (Figure 6, Item 30; Paragraph 8, Lines 2-7).

Concerning Claim 17, Mariaud discloses:

buffering the external power supply voltage to provide hysteresis for filtering noise (Figure 6, Item 30; Paragraph 8, Lines 2-7).

Concerning Claim 18, Mariaud discloses:

providing at least one transistor (Figure 6, Item 26) interconnected between the power source and the integrated circuit for controlling voltage on the input of the integrated circuit (Paragraph 6, Lines 1-6).

Concerning Claim 19, Mariaud discloses:

dropping the voltage of the power source before applying the voltage to the base of the at least one transistor (Paragraphs 1 and 5, Lines 8-10 and Lines 13 and 5-7, respectively).

Concerning Claim 22, Mariaud discloses:

The power supply source 26 is derived either from the voltage Vbus or from an external voltage Vdd at an input terminal 28 (Column 1, Lines 5-7).

Mariaud does not specifically disclose:

drawing relatively little current from the power source when the external power supply is at zero.

However, a USB device inherently will be current limited in the absence of an external power supply and thus the current drawn will be 'relatively little.'

Concerning Claim 25, Mariaud discloses:

A method for preventing malfunctions in a data transmission system which transmits digital signals along a data bus between a host computer and a peripheral device wherein the peripheral device may receive power from the host computer or alternatively from an external power source (Paragraph 5, Lines 5-7), comprising

interconnecting a transfer bridge circuit between the host computer and the peripheral device, the bridge circuit having a first interface between the bridge circuit and the host computer (Figure 6, Item 24), a second interface with a protective circuit (Figure 6, Item 26; the transistor serves as the protective circuit), and a third interface with the peripheral device electronics (The third interface is not shown, however interaction with further peripheral device electronics is inherent to the utility of the peripheral device),

providing a pull-up resistor connected in a separate line between the first interface and the data bus (Figure 1, Item Rr; Paragraph 4, Lines 1-3),

sensing whether power is being supplied along a power line from the host computer to the peripheral device (Figure 6, Item 60; Paragraph 24, Lines 5-7), and if appreciable power is not detected in the host power line (Paragraph 7, Lines 5-7), then

deactivating the pull-up resistor to prevent any malfunction from occurring (Paragraph 6, Lines 1-6).

Concerning Claim 29, Mariaud discloses:

providing an input line to the second interface from an electronic gate coupled to the power line (Figure 6, Items 72 and 74), and incorporating a logic circuit in the bridge

circuit connected to the second interface (Figure 6, Item 70), and generating a logical I/O control signal from the logic circuit to cause the enabling or disabling of the pull-up resistor (Paragraph 24, Lines 7-8).

Concerning Claim 30, Mariaud discloses:

said input line is capable of creating three different states of operation in the bridge circuit (Figure 4), including a first state when an external power supply is connected to the peripheral device with the pull-up resistor disabled (Paragraph 36, Lines 4-6).

Concerning Claim 31, Mariaud discloses:

the data bus incorporates two transmission lines each capable of transmitting data at different rates, respectively (Paragraph 4, Lines 3-6), and including a second state when the host computer supplies power to the peripheral device with the pull-up resistor enabled (Figure 4; Paragraph 36, Lines 4-6).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 13 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mariaud.

Concerning Claim 13, Mariaud discloses:

said application specific integrated circuit provides a NOR gate function and a NOT gate function for allowing current to flow to the pull-up resistor if the voltage on the input represent a logic one (Figure 6, Items 72 and 74).

Mariaud does not disclose the use of an AND gate to affect the current flow in this manner.

However, the use of an AND gate over a NOR and a NOT gate represents a design choice. Mariaud could have just as easily implemented the functionality described in his disclosure with the use of an AND gate by using the well-known concept of logical equivalence and still produced the same functionality described in his system.

Concerning Claim 23, Mariaud discloses:

said determining if the voltage on the input represents a logic one or a logic zero is performed by providing NOR gate and NOT gate functions between the input of the integrated circuit and the pull-up resistor such that the NOR gate and NOT gate functions will allow current to flow through the pull-up resistor if a logic one is present (Figure 6, Items 72 and 74).

Mariaud does not disclose the use of an AND gate to affect the current flow in this manner.

However, the use of an AND gate over a NOR and a NOT gate represents a design choice. Mariaud could have just as easily implemented the functionality described in his disclosure with the use of an AND gate by using the well-known concept of logical equivalence and still produced the same functionality described in his system.

17. Claims 2-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mariaud in view of Mughir.

Concerning Claim 2, Mariaud discloses:

A transistor for controlling the voltage to the input of the integrate circuit.

Mariaud does not disclose the specifics of the transistor implementation.

Mughir teaches:

said at least one transistor has a base, a collector and an emitter, the power source connected to the base, the external power supply connected to collector and the emitter connected to the integrated circuit (Column 4, Lines 21-27; although Mughir describes the connections of the transistor in terms of a FET, he states the FET may be replaced by a BJT, thus resulting in the transistor connections as described in the claim).

Mughir demonstrates that the BJT, which employs base, collector and emitter terminology, is a well-known method of implementing a voltage regulator. Accordingly, it would have been obvious to a person of ordinary skill in the art to implement the device described by Mariaud with the specific use of BJT transistors as taught by Mughir for the purposes of creating a voltage regulator.

Concerning Claim 3, Mughir further teaches:

including at least one first resistor interposed between the power source and the base of the at least one transistor to drop the voltage of the power source before being applied to the base of the at least one transistor (Figure 3, Item 343).

Concerning Claim 4, Mughir further teaches:

including a second resistor connected to ground and to the emitter of the at least one transistor (Figure 3, Item 329) and a first pull-up resistor connected between the external power supply and the emitter of said at least one transistor (Figure 3, Item 349).

Concerning Claim 5, Mariaud discloses:

the power source is at approximately 5 volts (Paragraph 2, Lines 8-10) and the external power supply is at approximately 3.3 volts (Paragraph 5, Lines 1-3).

Mariaud does not disclose:

the first resistor is an approximately 121 kOhm resistor, the second resistor is an approximately 2.49 kOhm resistor, and the transistor is a Q2N2222 transistor.

Mughir teaches:

Having a first and second resistor and a transistor to implement a voltage regulator. However, he does not provide the specific values or types of transistors needed to implement the device. The selection of the specific components described by Meghir may be left at the discretion of the circuit designer. Different components and component values may be substituted without changing the operation of the device.

Accordingly, it would have been obvious to a person of ordinary skill in the art to design the device described by Mariaud in view of Mughir using the specific resistor and transistor components as defined in the claim.

Concerning Claim 6, Mariaud discloses:

A transistor for controlling the voltage to the input of the integrate circuit.

Mariaud does not disclose the specifics of the transistor implementation.

Mughir teaches:

A transistor comprises an NPN bipolar junction transistor (Column 4, Lines 21-23; although Mughir does not explicitly define the bipolar junction transistor as being as specifically NPN, the connections described in the specification for a FET would, when replaced by a transistor as described in the specification be an NPN transistor; additionally, the functionality of a BJT, when connected correctly, will operate according to the teachings of the specification by using either an NPN or PNP BJT).

Mughir demonstrates that the BJT is a well-known method of implementing a voltage regulator. Accordingly, it would have been obvious to a person of ordinary skill in the art to implement the device described by Mariaud with the specific use of BJT transistors as taught by Mughir for the purposes of creating a voltage regulator.

18. Claims 12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mariaud in view of Smith.

Concerning Claim 12, Mariaud does not disclose:

said logic circuit is a universal serial bus to ATAPI bridge.

Smith teaches:

configuring the integrated circuit as a universal serial bus to ATAPI bridge (Column 5, Lines 34-38).

Smith is motivated to do this because "the USB logic 106 is a more compact design because less USB dedicated circuitry will be needed to carry out the USB data transfers" (Column 5, Lines 8-10).

Accordingly, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the voltage monitoring serial link disclosed by Mariaud with the teachings of a bridging USB circuitry with ATAPI components for the benefit of minimizing the costs and use of application specific circuitry.

Concerning Claim 20, Mariaud does not disclose:

Configuring the integrated circuit as a universal serial bus to ATAPI bridge.

Smith teaches:

configuring the integrated circuit as a universal serial bus to ATAPI bridge (Column 5, Lines 34-38).

Smith is motivated to do this because "the USB logic 106 is a more compact design because less USB dedicated circuitry will be needed to carry out the USB data transfers" (Column 5, Lines 8-10).

Accordingly, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the voltage monitoring serial link disclosed by Mariaud with the teachings of a bridging USB circuitry with ATAPI components for the benefit of minimizing the costs and use of application specific circuitry.

19. Claims 14, 24 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mariaud in view of *Logic Design Information*.

Concerning Claim 14, Mariaud discloses:

The use of logic gates to affect the state of a pull-up resistor (Figure 6, Items 72 and 74; Paragraph 26, Lines 8-10).

Mariaud does not disclose, however, the specific voltage thresholds representing logic ones and logic zeros to be 2.7 and 2.2 Volts, respectively.

Logic Design Information teaches that logic gates have voltage thresholds that vary depending on the circuitry used to implement the gates. For example, the Vil for CMOS is 1.3 and Vih is 3.7 Volts, respectively. These values vary from TTL and ETL families.

The use of 2.7 and 2.2 Volt levels to represent logical ones and zeros is clearly dependent upon the circuitry used within a system. Though Mariaud does not specify the actual voltage thresholds used by the disclosed logic gates, it would be obvious to a person of ordinary skill in the art to set thresholds to such levels should the logic circuitry require such voltage thresholds.

Concerning Claim 24, Mariaud discloses:

Enabling or disabling a pull-up resistor based upon the logic output from logic gates (Figure 6, Items 72and 74; Paragraph 26, Lines 8-10).

Mariaud does not disclose, however, enabling and disabling the pull-up resistor at the specific voltage thresholds of 2.7 and 2.2 Volts, respectively.

Logic Design Information teaches that logic gates have voltage thresholds that vary depending on the circuitry used to implement the gates. For example, the Vil for CMOS is 1.3 and Vih is 3.7 Volts, respectively. These values vary from TTL and ETL families. Logic gates implement an enable/disable functionality wherein the enable voltage and the disable voltage are distinct.

Logic gates provide an enable/disable functionality and *Logic Design Information* demonstrates that the voltage levels for this functionality is implementation specific. Though Mariaud does not specify the actual thresholds used by the disclosed logic gates, it would be obvious to a person of ordinary skill in the art to set these thresholds to such levels should the logic circuitry require it.

Concerning Claim 26, Mariaud discloses:

said deactivating occurs upon sensing that a voltage in the host power line is below a predetermined first threshold level (Paragraph 8, Lines 7-11).

Logic Design Information teaches that in binary logic, a voltage that is below a threshold value represents one logical value.

Concerning Claim 27, Mariaud discloses:

activating the pull-up resistor upon sensing that a voltage in the host power line is above a predetermined second threshold level (Paragraph 8, Lines 7-11).

Logic Design Information teaches that in binary logic, a voltage that is above a threshold value represents one logical value.

Concerning Claim 28, Mariaud discloses:

said second threshold level is higher than said first threshold level (Paragraph 8, Lines 7-11)

Logic Design Information teaches that the second threshold level is distinct from the first logic threshold level.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Technical Q&A HW82 describes developer information on the specifics of the problem that the claimed invention intends to resolve.

Power Macintosh G3 (Blue and White) and G4 serves as a technical article acknowledging the existence of the problem.

Monitoring the Vbus Signal for USB Self-Powered Devices describes the use of a STMicroelectronics circuit that will address the problem the claimed invention intends to resolve. It should be noted that the device described by Mariaud is assigned to STMicroelectronics.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew A. Henry whose telephone number is (571) 272-3845. The examiner can normally be reached on Monday - Friday (8:00 am -5:00 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER ~~2600~~ 2100

MAH